AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for the simultaneous storage and playback of multimedia data, comprising:

an input section for acquiring ~~and tuning~~ an input signal;

an output section, wherein said input signal is passed to said output section as a transport stream; said output section including:

a processor;

~~means for decoding~~ a decoder subsystem that decodes said transport stream, said ~~means for decoding said transport stream~~ decoder subsystem connected to said processor by ~~means of~~ a first data bus ~~transfer element~~; and

a ~~bridging element~~ media switch connected to said decoder subsystem ~~/host controller~~ by ~~means of~~ a second data bus ~~transfer element~~, said ~~bridging element~~ media switch operative to interface a plurality of system components and operates asynchronously from said processor.[[;]]

~~wherein said input section is individualized according to source type.~~

2. (Original) The system of Claim 1, wherein said input section is adapted to accept an analog input signal.

3. (Currently Amended) The system of Claim 2, wherein said input section accepts said analog input signal from any of: RF coaxial, composite audio/video ~~and~~ or S-video connectors.

4. (Currently Amended) The system of Claim 2, said input section comprising;

a tuner for ~~tuning to~~ selecting a desired channel;

a decoder for digitizing a video component of said input signal;

a ~~multi-standard~~ sound processor for processing an audio component of said input signal into a digitized audio component;

an MPEG-2 encoder, wherein said MPEG-2 encoder receives ~~said~~ digitized video and audio components, whereupon said digitized video and audio components ~~signals~~ are encoded and multiplexed into an MPEG-2 transport stream.

5. (Original) The system of Claim 4, further comprising a memory element.

6. (Currently Amended) The system of Claim 3, further comprising a secondary input, said secondary input comprising any of: a second set of RF coaxial, composite audio/video or S-video connectors.

7. (Original) The system of Claim 1, wherein said input section is adapted to accept a digital satellite input signal.

8. (Original) The system of Claim 7, wherein said input section comprises:

at least one satellite tuner; and

at least one demodulating element to demodulate the digital satellite signal to an MPEG-2 transport stream.

9. (Original) The system of Claim 1, wherein said input section is adapted to accept an input signal in both analog and digital formats from at least one RF coaxial connector.

10. (Currently Amended) The system of Claim 9, wherein said input section comprises:

at least one tuner for ~~tuning to~~ selecting a desired channel;

at least one decoder for digitizing a video component of said input signal;

at least one ~~multi-standard~~ sound processor for processing an audio component of said input signal into a digitized audio component;

an MPEG-2 encoder having multi-stream encode capability, wherein said MPEG-2 encoder receives said digitized video and audio components, whereupon said digitized video and audio components ~~signals~~ are encoded and multiplexed into an MPEG-2 transport stream.

11. (Original) The system of Claim 10, further comprising at least one memory element.

12. (Original) The system of Claim 1, said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section.

13. (Currently Amended) The system of Claim 12, said ~~means for decoding a transport stream~~ decoder further comprising an MPEG transport stream decoder/graphics subsystem~~, wherein said first data transfer element comprises a host bus~~.

14. (Currently Amended) The system of Claim 13, wherein said MPEG transport stream decoder/graphics subsystem includes any combination of:

a host bridge;

a memory controller;

an MPEG-2 transport demultiplexer;

an MPEG-2 decoder;

an audio/video decoder;

a graphics processor;

a ~~PCI~~ bus bridge; or

a bus controller[[;]] .

~~a SMARTCARD interface; and~~

~~a modem interface.~~

15. (Currently Amended) The system of Claim 14, said MPEG transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section.

16. (Currently Amended) The system of Claim 14, wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back through an output side of said MPEG transport stream decoder/graphics subsystem.

17. (Currently Amended) The system of Claim 14, wherein said MPEG transport stream decoder/graphics subsystem further comprises a plurality of outputs, wherein said decoded ~~signal~~ transport stream is output to a television, said outputs including any of:

S-video;

audio;

SPDIR (Stereo Paired Digital Interface); ~~and~~ or

CVBS (Composite Video Baseband Signal).

18. (Currently Amended) The system of Claim 14, further comprising a SMARTCARD interface and at least one SMARTCARD reader interfaced to said MPEG transport stream decoder/graphics subsystem.

19. (Currently Amended) The system of Claim 14, further comprising a flash PROM connected to said transport stream decoder/graphics subsystem, said PROM containing boot code that initializes said system prior to loading of an operating system kernel.

20. (Original) The system of Claim 14, further comprising a SDRAM connected to said transport stream decoder/graphics subsystem.

21. (Canceled)

22. (Currently Amended) The system of Claim 1, wherein said processor comprises a MIPS processor ~~and wherein said first data transfer element comprises a host bus~~.

23. (Original) The system of Claim 1, wherein said processor is operative to run system software, middleware, and application software.

24. (Original) The system of Claim 23, wherein said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.

25. (Currently Amended) The system of Claim 1, wherein said ~~bridging element~~ media switch comprises a media manager, said media manager including:

a[[n]] ~~IDE~~ host controller ~~with data encryption~~;

a DMA controller;

~~an IR receiver/transmitter interface;~~

~~at least one UART (Universal Asynchronous Receiver/Transmitter);~~

~~at least one I^2S bus;~~

~~at least one GPIO (General Purpose Input/Output);~~

a ~~PCI~~ bus arbiter; and

an MPEG media stream processor[[;]] .

~~a PCM audio mixer (Pulse Code Modulation);~~

~~a high speed transport output interface;~~

~~a fan control; and~~

~~a scanning interface for a front panel navigation keypad cluster.~~

26. (Original) The system of Claim 25, wherein said media manager is implemented in an ASIC (Application Specific Integrated Circuit) or a programmable logic device.

27. (Canceled)

28. (Canceled)

29. (Currently Amended) The system of Claim 25, further comprising a real-time clock connected to ~~said~~ an I^2S bus.

30. (Currently Amended) The system of Claim 25, further comprising a secure micro controller connected to ~~said~~ a UART (Universal Asynchronous Receiver/Transmitter) included in said media manager, said micro controller operative in cryptographic applications, including authentication and encryption/decryption.

31. (Currently Amended) The system of Claim 25, further comprising a RS232 port coupled to ~~said~~ a UART (Universal Asynchronous Receiver/Transmitter) included in said media manager.

32. (Original) The system of Claim 25, further comprising a IEEE1394 interface integrated on said media manager.

33. (Currently Amended) The system of Claim 25, further comprising a front panel LED array coupled to ~~said~~ a GPIO (General Purpose Input/Output) included in said media manager.

34. (Currently Amended) The system of Claim 25, further comprising a front panel navigation cluster coupled to ~~said~~ a GPIO (General Purpose Input/Output) included in said media manager.

35. (Currently Amended) The system of Claim 25, further comprising a remote control coupled to ~~said~~ an IR receiver/transmitter interface included in said media manager.

36. (Currently Amended) The system of Claim 1, wherein said second ~~data transfer~~ bus element comprises a system bus.

37. (Original) The system of Claim 36, wherein said system bus comprises a PCI bus.

38. (Original) The system of Claim 37, further comprising a USB (Universal Serial Bus) controller coupled to said PCI bus.

39. (Original) The system of Claim 1, wherein said system is implemented as a system board.

40. (Currently Amended) The system of Claim 1, wherein said output section is implemented as a plurality of microchips, the microchips connected to each other by ~~means of~~ said ~~data transfer~~ first and second bus elements.

41. (Original) The system of Claim 1, wherein said output section is implemented as either a single microchip or a chipset.

42. (Withdrawn) A system for processing a media stream across several channels simultaneously, comprising:

means for observing a data stream on a data bus;

means for identifying media streams within said data stream;

means for associating media stream data objects with their respective media streams;

a multi channel media stream processor, wherein said media processor processes media stream data across a plurality of channels, in parallel; and

means for monitoring and saving state of said processor as said processor switches from an original media stream to a next media stream, wherein, if said processor switches back to said original stream, a state associated with said original stream is reloaded.

43. (Withdrawn) The system of Claim 41, wherein said means for observing said data stream comprises a system interface, said system interface comprising a passive, slave client on said bus, wherein said system interface observes said data stream without interfering with data flow.

44. (Withdrawn) The system of Claim 43, wherein said system interface is individualized to a particular system type, said individualization being accomplished by one of: programmable switches and hardwiring.

45. (Withdrawn) The system of Claim 43, wherein said data bus is one of: a system bus and a memory bus.

46. (Withdrawn) The system of Claim 42, wherein said means for identifying a media stream comprises a media stream identifier, wherein said media stream distinguishes media streams from the remainder of said data stream according to source and destination addresses.

47. (Withdrawn) The system of Claim 42, wherein said means for associating media data objects with their respective media streams comprises a media identification generator, said media identification generator assigning tags to media stream data objects, so that any data object is associated with its stream of origin.

48. (Withdrawn) The system of Claim 42, wherein said means for monitoring and saving state of said processor comprises a multi-channel state engine, said state engine monitoring media stream identifiers, and saving said processor state, said saved state comprising a first state, when a media stream identifier associated with said next media stream is associated.

49. (Withdrawn) The system of Claim 48, wherein said state engine reloads the first state if a media stream identifier associated with said first state is presented.

50. (Withdrawn) The system of Claim 42, further comprising a media stream data structure, said processed media stream being saved to said data structure and routed to system memory as needed.

51. (Withdrawn) The system of Claim 42, wherein said system is implemented in a programmable logic device.

52. (Withdrawn) A method of processing a media stream across several channels simultaneously, comprising the steps of:

observing a data stream on a data bus;

identifying media streams within said data stream;

associating media stream data objects with their respective media streams;

processing media stream data across a plurality of channels, in parallel; and

monitoring and saving a media processor state as said processor switches from an original media stream to a next media stream; and

reloading state associated with said original stream if said processor switches back to said original stream.

53. (Withdrawn) The system of Claim 52, wherein said step of observing said data stream comprises the steps of:

providing a system interface, said system interface comprising a passive, slave client on said bus; and

said system interface observing said data stream without interfering with data flow.

54. (Withdrawn) The system of Claim 53, wherein said system interface is individualized to a particular system type, said individualization being accomplished by one of: programmable switches and hardwiring.

55. (Withdrawn) The system of Claim 53, wherein said data bus is one of: a system bus and a memory bus.

56. (Withdrawn) The system of Claim 52, wherein said step of identifying a media stream comprises the steps of:

distinguishing media streams from the remainder of said data stream according to source and destination addresses.

57. (Withdrawn) The method of Claim 52, wherein said step of:

associating media data objects with their respective media streams comprises:

assigning tags to media stream data objects, so that any data object is associated with its stream of origin.

58. (Withdrawn) The method of Claim 52, wherein said step of monitoring and saving said processor state comprises the steps of:

monitoring media stream identifiers; and

saving said processor state, said saved state comprising a first state, when a media stream identifier associated with said next media stream is associated.

59. (Withdrawn) The method of Claim 58, wherein said step of monitoring and saving said processor state further comprises:

reloading the first state if a media stream identifier associated with said first state is presented.

60. (Withdrawn) The method of Claim 52, further comprising the steps of:
saving said processed media stream to a media data structure; and
routing to system memory as needed.

61. (Withdrawn) The method of Claim 52, said method implemented by means of a programmable logic device.